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NOTICE OF ALLOWANCE AND FEE(S) DUE

20792 7590 04/02/2008

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER

IM, JUNGHIWA M

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 04/02/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/689,976

10/21/2003

Glenn A. Rinne

9180-24

3798

TITLE OF INVENTION: STACKED ELECTRONIC STRUCTURES INCLUDING OFFSET SUBSTRATES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$300	\$0	\$1740	07/02/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20792 7590 04/02/2008

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RALEIGH, NC 27627

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,976	10/21/2003	Glenn A. Rinne	9180-24	3798

TITLE OF INVENTION: STACKED ELECTRONIC STRUCTURES INCLUDING OFFSET SUBSTRATES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$300	\$0	\$1740	07/02/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
IM, JUNGHWA M	2811	257-686000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,976	10/21/2003	Glenn A. Rinne	9180-24	3798
20792	7590	04/02/2008	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			IM, JUNGHWAM	
			ART UNIT	PAPER NUMBER
			2811	
DATE MAILED: 04/02/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 408 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 408 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/689,976

Applicant(s)

RINNE, GLENN A.

Examiner

JUNGHWA M. IM

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed 01/08/2008.
2. ☒ The allowed claim(s) is/are 2-4,6-19,21-31,33-40,42-52,55-60 and 62-79.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other ____. |

/Lynne A. Gurley/SPE

DETAILED ACTION

Allowable Subject Matter

Claims 2-4, 6-19, 21-31, 33-40, 42-52, 55-60, and 62-79 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of "a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate" and "wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate," or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, in particular a first electrical and mechanical connection between the first and third integrated circuit substrates bypasses the second integrated circuit substrate and a conductive trace (or a conductive bump) on a surface of the first integrated circuit substrate provides an electrical coupling between the first and third electrical and mechanical connections, or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, in particular a first electrical and mechanical connection between the first and third integrated circuit substrates bypasses the second integrated circuit substrate and a conductive trace (a conductive bump) on a

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surface of the first integrated circuit substrate provides an electrical coupling between the first and third electrical and mechanical connections, or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of “a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates” and “wherein the first, second, third, fourth and fifth conductive bumps comprise portions of a signal path, wherein a direct electrical coupling is provided between the signal path and an electronic circuit of the fifth integrated circuit substrate, and wherein the signal path is free of a direct electrical coupling with any electronic circuit of the third integrated circuit substrate,” or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of “wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond a first end of the second integrated circuit substrate wherein a second end of the second integrated circuit substrate extends beyond the first and third integrated circuit substrates wherein each of the first, second, and third integrated circuit substrates is on a same side of the printed circuit board and wherein each of the first, second, and third

integrated circuit substrates has a device side facing the printed circuit board and a backside facing away from the printed circuit board," or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of " wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate" and "the device side of each of the first, second, and third integrated circuit substrates faces the printed circuit board and the backside of each of the first, second, and third integrated circuit electronic devices faces away from the printed circuit board," or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of "a signal path extending along a first conductive trace on the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along a second conductive trace on the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along a third conductive trace on the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate" or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of "a signal path extending along the first surface of the second integrated circuit substrate, to the

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second surface of the first integrated circuit substrate, along the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate” and “wherein the signal path further extends along the second surface of the second integrated circuit substrate, and to a first surface of the fourth integrated circuit substrate” or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of “a second array of interconnection structures on the second surface of the substrate wherein the second array of interconnection structures are arranged in a second pattern and wherein the second pattern is a mirror image of the first pattern wherein the substrate comprises an integrated circuit substrate such that the first surface is a device side of the substrate having electronic circuits thereon and the second surface is a backside of the device” or

Prior art fails to teach or render obvious, either singularly or with combinations of elements as set forth in the claims including, at least the limitation of “wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond a first end of the second integrated circuit substrate wherein a second end of the second integrated circuit substrate extends beyond the first and third integrated circuit substrates wherein the first, second, and third integrated circuit substrates are configured to be mounted on a same side of a printed circuit board so that device sides of the first, second, and third integrated circuit substrates face the printed circuit board

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and so that backsides of the first, second, and third integrated circuit substrates face away from the printed circuit board.”

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/JMI/
3/28/2008